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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,656	03/29/2004	Jiaw-Ren Shih	252016-3090	2449

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EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/811,656	SHIH ET AL.	
	Examiner	Art Unit	
	Ajay K. Arora	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/12/2006 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.**

Claims 1, 4, 8 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Baudouin (US 6,373,127), hereinafter Baudouin.

Regarding Claim 1, Baudouin (refer to Figure 6a) teaches an integrated circuit (IC) comprising:

a primary substrate (61,66) having a top surface, a bottom surface and a plurality of side surfaces;

a plurality of contacts (connected to 68) on the top surface of the primary substrate (61,66) connectable to pins (64) of a packaging element; and

a capacitive coating (65) directly contacting at least the bottom surface of the primary substrate (61,66) to make contact with a lead frame (62) intended to secure the primary substrate to the packaging element.

Regarding Claim 8, Baudouin (refer to Figure 6a) teaches an electronic device comprising:

a packaging element having a number of pins (64) to externally connect the electronic device;

an integrated circuit (61,66) having a top surface, a bottom surface, and a plurality of side surfaces;

a plurality of contacts (connected to 68) on the top surface of the IC and connected to the pins (64) of the packaging element;

a capacitive coating (65) directly contacting at least the bottom surface of the IC (61,66); and

a lead frame (62) to secure the IC to the packaging element, the capacitive coating (65) sandwiched between the IC (61) and the lead frame (62).

Regarding claims 4 and 11, Baudouin teaches that the capacitive coating is a capacitive dielectric (Col. 4, lines 24-32 and 63-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

Claims 2, 3, 5-7, 9, 10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baudouin.

Regarding Claims 2 and 9, Baudouin teaches substantially the claimed structure, but does not specifically state that the capacitive coating has a capacitance that is "lower than an internal capacitance of the IC". However, Baudouin teaches that the parameters controlling capacitance may be modified to achieve a designated capacitance to suit a specific application (Col. 7, lines 34-36). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the device of Baudouin such that the capacitive coating has a capacitance that is lower than an internal capacitance of the IC. The ordinary artisan would have been motivated to

modify Baudouin for at least the purpose of achieving a lower effective capacitance (when two capacitors are connected in series, the resulting effective capacitance is lower than capacitance of either of the capacitors).

Regarding Claims 3 and 10, Baudouin (refer to Figure 6a) teaches that the capacitive coating extends from the bottom surface to the plurality of side surfaces (at least to the edges of side surface that are common with the bottom surface) of the primary substrate.

Further, note that it is well known in the art that the capacitance of a parallel plate capacitor is governed by the formula:

$$C = \epsilon_0 \epsilon_r \frac{A}{d}$$

where

C is the capacitance in in farads, F

ε_o is the permittivity of free space, measured in farads per meter

ε_r is the dielectric constant or relative permittivity of the insulator used

A is the area of each plane electrode, measured in square metres

d is the separation between the electrodes (or thickness of dielectric between the capacitor plates), measured in meters

It is clear from the above formula that capacitance is substantially independent of any dielectric that extends outside the area (A in above formula) to the side surfaces of the substrate/IC; i.e. the claimed device would have capacitance substantially the same as the device where dielectric does not extend to the side surfaces (also acknowledged in applicant's specification). Therefore, alternatively, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the device of Baudouin so as to allow the capacitive coating extending from the bottom surface to the plurality of side surfaces of the primary substrate/IC. The ordinary artisan would have been motivated to modify Baudouin for at least the purpose of achieving cost savings resulting from not having to reject parts if capacitive coating inadvertently extends to the side surfaces.

Regarding Claims 6, 7, 13 and 14, Baudouin teaches substantially the claimed structure, but does not specifically state that the capacitive coating has a thickness of "between 0.01 millimeters and 1.0 millimeters" (for claims 6 and 13), or "substantially 0.1 millimeters" (for claims 7 and 14). As shown in the above stated formula for capacitance, C, the capacitive coating thickness (d in the above formula) is merely a design parameter and further Baudouin teaches that thickness is one of the variables that may be varied to achieve a desired capacitance (Col. 4, lines 24-32). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the device of Baudouin such that the capacitive coating has a thickness of "between 0.01 millimeters and 1.0 millimeters" (for claims 6 and 13), or "substantially 0.1 millimeters"

(for claims 7 and 14). The ordinary artisan would have been motivated to modify Baudouin for at least the purpose of achieving a specific value of capacitance (Col. 4, lines 24-32).

Claims 1, 4, 8 and 11 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Bissey (US 6,054,754), hereinafter Bissey, in view of Baudouin.

Regarding Claim 1, Bissey (refer to Figure 1) teaches an integrated circuit (12) comprising:

a primary substrate having a top surface (16), a bottom surface (36), and a plurality of side surfaces;

a plurality of contacts (14) on the top surface (16) of the primary substrate connectable to pins (28 or 30) of a packaging element (20); and

a capacitive coating (32) contacting (via intervening members 22 and 40) at least the bottom surface (36) of the primary substrate to make contact with a lead frame (22A) intended to secure the primary substrate to the packaging element.

However, Bissey does not teach that the capacitive coating is "directly" contacting at least the bottom surface of the primary substrate. Baudouin teaches an integrated circuit with a primary substrate and a capacitive coating, wherein the capacitive coating (65) is directly contacting at least the bottom surface of the primary substrate (61,66). It would have been obvious to one of ordinary skills in the art at the time of the invention

to modify the device of Baudouin such that the capacitive coating is "directly" contacting at least the bottom surface of the primary substrate. The ordinary artisan would have been motivated to modify Baudouin for at least the purpose of achieving a lower cost structure if a single capacitor was required unlike Bissey which is optimized for multiple capacitors capable of working across multiple frequencies (see Bissey, Col. 3, lines 58-67).

Regarding Claim 8, Bissey (refer to Figure 1) teaches an electronic device comprising:

a packaging element (20) having a number of pins (28 or 30) to externally connect the electronic device;

an integrated circuit (12) having a top surface (16), a bottom surface (36), and a plurality of side surfaces;

a plurality of contacts (14) on the top surface (16) of the IC (12) and connected to the pins (28 or 30) of the packaging element (20);

a capacitive coating (32) contacting (via intervening members 22 and 40) at least the bottom surface (36) of the IC (12); and,

a lead frame (22A) to secure the IC to the packaging element, the capacitive coating (32) sandwiched between the IC (12) and the lead frame (22A).

However, Bissey does not teach that the capacitive coating is "directly" contacting at least the bottom surface of the IC. This limitation has already been addressed in the rejection of claim 1 abobe in view of Baudouin.

Regarding claim 4 and 11, Bissey teaches that the capacitive coating (32) is a capacitive dielectric (Col. 3, lines 50-55).

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bissey (US 6,054,754), hereinafter Bissey, in view of Baudouin.

Regarding Claims 5 and 12, Bissey teaches substantially the claimed structure, but does not specifically state that the capacitive dielectric has "a low k value". However, Bissey teaches that the k value (i.e. dielectric constant value) of the dielectric may vary widely and may be tailored to suit particular requirements (Col. 5, lines 29-32). Since applicant had completely failed to disclose the composition or material of the capacitive coating, the above teaching encompasses all well known dielectrics and corresponding k values – high, low or anything therebetween. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify the device of Bissey such that the capacitive dielectric has "a low k value". The ordinary artisan would have been motivated to modify Bissey for at least the purpose of achieving a low capacitance for a given thickness of the dielectric, since capacitance is directly proportional to dielectric constant (referred to as "k value" in claims) of the dielectric.

Response to Arguments

Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ajay K. Arora whose telephone number is (571) 272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sara Crane
Primary Examiner